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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,910	01/29/2004	Dirk Manger	INF-131	2648

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EXAMINER	
LUU, CHUONG A	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/765,910	MANGER, DIRK
	Examiner	Art Unit
	Chuong A. Luu	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *19 and 20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/13/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election of Group I, claims 1-18 in the reply filed on July 22, 2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The Rejections

Claims 1-10 and 13-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Nowad (U.S. 6,610,576 B2).

Nowak discloses a transistor with

(1) providing at least one original fin (56) made of a semiconductor material on a substrate by means of a first lithography step,

providing a gate dielectric layer (58) on the longitudinal sides of the at least one original fn (56),

providing a gate electrode layer (54) made of a conductive gate electrode material on the gate dielectric layer (58);

forming contact trenches (62) that pattern the at least one original fn (56) in a longitudinal direction by means of a second lithography step, wherein at least one transistor fin with a first head end and a second head end at a distance of a fin length from the latter emerges from the at least one original fin (56), and wherein a gate electrode (54) associated with the transistor fin emerges from the gate electrode layer (54);

processing the gate electrode (54), wherein the gate electrode recedes from both head ends (see Figure 1);

(2) further comprising: forming a source/drain region in the transistor fin from the two head ends; and connecting the source/drain regions to source/drain contact structures made of a conductive contact material, wherein the gate electrode material recedes from both head ends except for a controllable channel length (see Figure 1);

(3) wherein, by means of the first lithography step, a plurality of original fins which are arranged next to one another and nm parallel are formed and the gate electrode layer is pre-patterned before the formation of the gate electrodes, and wherein the gate electrode layer in a bottom region of trenches formed between the original fns is subdivided into sections that are separated from one another and in each case associated with one of the original fns (see Figure 1);

(4) wherein the gate electrode layer essentially emerges from a conformal deposition, and wherein the pre-patterning of the gate electrode layer comprises: providing a nonconformalmask, by which at least the gate electrode mateeria bearing on the original fns is covered, and at least the bottom region of the trenches is in each case left free; removing sections of the gate electrode layer from the bottom regions not covered by the mask (see Figure 1);

(5) wherein the providing the nonconformal mask comprises: depositing a nonconformal mask material, wherein the mask material is deposited with a smaller layer thickness in the bottom region of the trenches than on the original fins; and causing the mask material to recede, so that the mask material is removed from the bottom region of the trenches and remains on the original fins (see Figure 1);

(6) wherein the nonconformal mask is removed after the pre-patterning of the gate electrode layer (see Figure 1);

(7) wherein after the pre-patterning of the gate electrode layer and before the second lithography step, a first isolating dielectric is applied to a pre-patterned gate electrode layer (see Figure 1);

(8) wherein the contact trenches are introduced in the course of the second lithography step by means of a nonselective etching step (see Figure 1);

(9) wherein the process of causing the gate electrode to recede comprises an etching step which causes the gate electrode material to selectively recede (see Figure 1);

(10) wherein doped polysilicon is provided as gate electrode material (see Figure 1);

(13) wherein the source/drain regions are produced in the transistor tin by means of implantation (see Figure 1);

(14) wherein the contact trenches are lined at least partly by an isolating coating, wherein all of the conductive sections adjoining the respective contact trench are covered by means of the isolating coating, with the exception in each case of a source/drain region adjoining one of the contact trenches (see Figure 1);

(15) wherein the isolating coating is applied conformally and subsequently patterned on one side (see Figure 1);

(16) wherein the etching resistance of the isolating coating is altered on one side by means of inclined implantation, and wherein an etching that is selective relative to altered and unaltered sections of the isolating coating is subsequently carried out;

(17) wherein the contact trenches are filled with conductive material (see Figure 1);

(18) wherein a geometrical channel length of a channel region formed between the two source/drain regions is provided, such that the geometrical channel length is greater than or equal to a controllable channel length (see Figure 1).

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nowad (U.S. 6,610,576 B2) in view of Fried et al. (U.S. 6,583,469 B1).

Nowak teaches everything above except for wherein the gate electrode material is caused to recede by means of an etching step in a Cl plasma or an HBr plasma; wherein divots produced as a result of the gate electrode material having been caused to recede are filled with a filling material. However, Fried discloses a FET with **(11)** wherein the gate electrode material is caused to recede by means of an etching step in a C1 plasma or an HBr plasma (see column 4, lines 35-41); **(12)** wherein divots produced as a result of the gate electrode material having been caused to recede are filled with a filling material (see Figure 7B). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Nowak's device (accordance with the teaching of Fried) by selecting etching step in a Cl plasma or an HBr plasma and wherein divots produced as a result of the gate electrode material having been caused to recede are filled with a filling material since it has been held that mere duplication of the essential working parts of a device involves only

routine skill in the art. Doing so would facilitate the manufacture of the semiconductor device and improve the speed of the semiconductor structure.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chuong Anh Luu
Patent Examiner
September 23, 2005